REMARKS

Claims 1-11 are pending in the application; the status of the claims is as follows:

Claims 1-3, 8, and 11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication No. 2002/0057351 to Suzuki et al. (hereinafter "Suzuki et al") in view of U.S. Patent No. 6,380,975 to Suzuki (hereinafter "Suzuki").

Claims 4-7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Published Application No. 2001/0001563 to Tomaszewski (hereinafter "Tomaszewski"), in view of WO 99/40723 to Clemens (hereinafter "Clemens") in view of Suzuki et al and further in view of U.S. Patent No. 6,567,122 to Anderson et al. (hereinafter "Anderson").

Claims 9 and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Suzuki et al in view of Suzuki and further in view of U.S. Patent No. 6,278,492 to Nakamura (hereinafter "Nakamura").

Claims 1, 4, 8, and have been amended to clarify that the camera includes reconfigurable logic circuitry which may be selectively configured to perform different image processing functions by loading different program into the logic circuitry. Claim 4 has been amended to improve the form thereof. These changes do not introduce any new matter.

35 U.S.C. § 103(a) Rejections

The rejection of claims 1-3, 8, and 11 under 35 U.S.C. § 103(a), as being unpatentable over Suzuki et al in view of Suzuki, is respectfully traversed because there is no motivation or suggestion to combine the cited references as proposed and because the proposed combination fails to teach all of the features found in the claims.

Suzuki et al, teaches an electronic camera "capable of recording image, voice, text, line-drawn information, and the like." *See* Abstract. The camera includes CPU 34 which may be implemented using "a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit elements, an ASIC or other integrated circuit elements, a hardwired electronic or logic circuit such as a discrete element circuit, a programmable logic device such as a PLD, PLA, FGPA or PAL, or the like. In general, any device on which a finite state machine capable of implementing the flowchart shown in FIG. 3 can be used to implement the CPU 34." See Fig. 4 and paragraph [0054]. Suzuki et al provides no other teaching with regard to reconfigurable logic elements. In particular, Suzuki et al teaches that special purpose circuits are used for image processing functions. For example, compression and expansion memory controller (CEMC) circuit 38 compresses image data before it is recorded to memory card 24 and decompresses compressed image data on memory card 24 for display on LCD 6. See paragraphs [0064] and [0087].

Suzuki teaches a "digital still camera that records both images and voice." *See* Abstract. The camera includes "... a DCT (Discrete Cosine Transform) 108 for executing D/A conversion which is a step of image compression/extension based on the JPEG standard; a coder (Huffman Encoder/Decoder) 109 for executing encoding and decoding each as a process of the image compression/expression based on the JPEG standard; an MCC 110 (Memory Card Controller) for ... recording the data in or reading the data from the memory card 103; an ADPCM (Adaptive Differential Pulse Code Modulation) 112 for converting voice inputted through the microphone 111 to digital data ...; [and] a CPU 113 for controlling each of the sections described above ...." Thus, Suzuki also teaches the use of special purpose circuits for performing image processing functions. Suzuki provides no teaching whatsoever about the use of reconfigurable circuitry for performing image processing.

Neither Suzuki et al., or Suzuki disclose, teach, or otherwise suggest that a reconfigurable processing element may be used for anything other than implementing the

CPU. Therefore, the references can not provide any motivation to modify the camera of Suzuki as suggested in the Office Action. Accordingly, the combination is improper.

Moreover, even assuming the combination were proper, *arguendo*, the combination still fails to teach all elements of the rejected claims. For example, claim 1 recites *inter alia*:

> "...an electronic circuit arrangement in which a logic circuit is obtained when a predetermined program is written, said logic circuit is configured depending on the written program, and said logic circuit executes a predetermined operation on inputted image data,
>
> a memory for memorizing a first program corresponding to the first image data processing and a second program corresponding to the second image data processing; and
>
> a controller for reading the first program from the memory and writing it in the electronic circuit arrangement when the first mode is selected by the mode selector and for reading the second program from the memory and writing it in the electronic circuit arrangement when the second mode is selected by the mode selector."

Thus, claim 1 requires a memory in which are stored programs corresponding to different image data processing operations, an electronic circuit that performs the different image processing operations depending on what program is loaded therein, and a controller for transferring the programs from the memory to the electronic circuit. It is respectfully submitted that none of the cited references teach these elements of claim 1. Accordingly, claim 1 distinguishes the combination of Suzuki et al and Suzuki.

Claims 2 and 3 depend from claim 1. It is respectfully submitted, therefore, that claims 2 and 3 distinguish over the combination of Suzuki et al and Suzuki for at least the same reasons as provided above in regards to claim 1.

Claim 8 recites *inter alia*:

> "an electronic circuit arrangement in which a logic circuit is obtained when a predetermined program is written, said logic circuit is

configured depending on the written program, and said logic circuit executes a predetermined operation on image data input thereto;

a memory for memorizing a plurality of programs corresponding to the plurality of image processing; and

a controller for reading a program corresponding to the image processing selected by the image processing selector and writing it in the electronic circuit arrangement.

Thus, claim 8 requires a memory in which are stored programs corresponding to a plurality of image processing operations, an electronic circuit that performs the different image processing operations depending on what program is loaded therein, and a controller for transferring a selected program from the memory to the electronic circuit. It is respectfully submitted that as applied to claim 1 above, none of the cited references teach these elements of claim 8. Accordingly, claim 8 distinguishes the combination of Suzuki et al and Suzuki.

Claim 11 depends from claim 8. It is respectfully submitted, therefore, that claim 11 distinguishes over the combination of Suzuki et al and Suzuki for at least the same reasons as provided above in regards to claim 8.

Accordingly, it is respectfully requested that the rejection of claims 1-3, 8, and 11 under 35 U.S.C. § 103(a) as being unpatentable over Suzuki et al in view of Suzuki, be reconsidered and withdrawn.

The rejection of claims 4-7 under 35 U.S.C. § 103(a) as being unpatentable over Tomaszewski in view of Clemens in view of Suzuki and further in view of Anderson, is respectfully traversed because there is not motivation or suggestion to make the combination and because the combination fails to teach the elements of the rejected claims.

Tomaszewski teaches digital camera 104 configured to support both portable and tethered operating modes. Paragraph [0018]. Digital camera 104 periodically polls for USB connectivity by detecting the presence of a VBUS signal on the USB port.

Paragraph [0030]. If the VBUS signal is present, the tethered mode of operation is activated. If, on the other hand, the VBUS signal is not detected, the portable mode is activated. Paragraph [0033] Thus, Tomaszewski merely teaches that camera 104 detects whether the camera is connected to a host computer. It is respectfully submitted, however, that Tomaszewski does not teach that camera 104 detects "a *kind* of data communication standard of an equipment connected to the connection portion" as alleged at page 6 of the Office Action.

Clemens teaches a method and apparatus for capturing a still image during video streaming operations of a digital camera tethered to a computer system. Page 2, Summary of the Invention. Preferably, the camera is coupled to a general purpose computer using a USB communications interface. "Alternatively, other communications interfaces between a computer system and computer peripherals may be used." Page 5. The other communication interfaces may be, for example, "the RS-232 serial interface, the Universal Serial Bus (USB), or the higher performance Institute of Electrical and Electronics Engineers (IEEE) Standard 1394-1995." Page 8. Thus, Clemens teaches that a digital camera may include an interface for communicating using a standard protocol. However, it is respectfully submitted that Clemens does not teach that the camera may selectively use a first protocol to communicate with a first computer and a second different protocol to communicate with a second computer as alleged at page 7 of the Office Action.

As discussed above in connection with claim 1, Suzuki et al teaches that overall operation of a digital camera is controlled by a CPU which may be "a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit elements, an ASIC or other integrated circuit elements, a hardwired electronic or logic circuit such as a discrete element circuit, a programmable logic device such as a PLD, PLA, FGPA or PAL, or the like." Paragraph [0054].

Anderson teaches a "method for making a digital camera and its internally stored images remotely accessible," *e.g.*, "via the internet." Summary of the Invention

Claim 4 recites *inter alia*:

> "a connection portion to which a first equipment and a second equipment can alternatively be connected, the first equipment being communicative with the camera by a first data communication standard, and the second equipment being communicative with the camera by a second data communication standard;
>
> a detector for judging a kind of data communication standard of an equipment connected to the connection portion;
>
> an electronic circuit arrangement in which a logic circuit is obtained when a predetermined program is written, said logic circuit is configured depending on the written program, and said logic circuit executes a predetermined operation on inputted image data;
>
> a memory for memorizing a first program corresponding to a first image data communication processing fitting for the first data communication standard and a second program corresponding to a second image data communication processing fitting for the second data communication standard; and
>
> a controller for reading the first program from the memory and writing it in the electronic circuit arrangement when the kind of the data communication standard of the equipment connected to the communication portion is judged as the first data communication standard by the detector and for reading the second program from the memory and writing it in the electronic circuit arrangement when the kind of the data communication standard of the equipment is judged as the second data communication standard."

Thus, claim 4 requires a camera capable communicating using multiple communication standards and having a detector that determines what kind of communication standard is being used; a memory in which are stored programs corresponding to different image data processing operations apropos to the different data communication standards; an electronic circuit that performs the different image processing operations depending on what program is loaded therein, and a controller for transferring a selected program from the memory to the electronic circuit in response to the detector.

As discussed herein above, Tomaszewski fails to teach detecting a kind of data communication; Clemens fails to teach a camera that may selectively use any one of several communication protocols; Suzuki et al fails to teach a reconfigurable circuit that performs different processing based on a program loaded therein; and Anderson fails to

teach a memory for storing multiple programs for a reconfigurable circuit. None of the cited references make up for the noted defects. Moreover, none of the cited references teach a controller that transfers a selected program from the memory to the reconfigurable circuit. Accordingly, it is respectfully submitted that the proposed combination of references fails to teach all elements of claim 4, and claim 4 distinguishes over the combination.

Claims 5-7 depend from claim 4. It is respectfully submitted, therefore, that claims 5-7 distinguishes over the combination of Tomaszewski, Clemens, Suzuki, and Anderson for at least the same reasons as provided above in regards to claim 4.

Accordingly, it is respectfully requested that the rejection of claims 4-7 under 35 U.S.C. § 103(a) as being unpatentable over the Tomaszewski application in view of the Clemens patent in view of the Suzuki '351 patent and further in view of the Anderson patent, be reconsidered and withdrawn.

The rejection of claims 9 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Suzuki et al in view of Suzuki and further in view of Nakamura, is respectfully traversed because there is not motivation or suggestion to make the combination and because the combination fails to teach the elements of the rejected claims.

Claims 9 and 10 depend from claim 8. As provided herein above, claim 8 distinguishes over the combination of Suzuki et al and Suzuki. It is respectfully submitted that Nakamura adds nothing to the teachings of Suzuki et al and Suzuki that would cure the deficiencies noted therein. Therefore, claims 9 and 10 distinguishes over the combination of for at least the same reasons as provided above in regards to claim 8.

Accordingly, the rejection of claims 9 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Suzuki et al in view of Suzuki and further in view of Nakamura, be reconsidered and withdrawn.

CONCLUSION

Wherefore, in view of the foregoing amendments and remarks, this application is considered to be in condition for allowance, and an early reconsideration and a Notice of Allowance are earnestly solicited.

This Amendment does not increase the number of independent claims, does not increase the total number of claims, and does not present any multiple dependency claims. Accordingly, no fee based on the number or type of claims is currently due. However, if a fee, other than the issue fee, is due, please charge this fee to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260.

Any fee required by this document other than the issue fee, and not submitted herewith should be charged to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260. Any refund should be credited to the same account.

If an extension of time is required to enable this document to be timely filed and there is no separate Petition for Extension of Time filed herewith, this document is to be construed as also constituting a Petition for Extension of Time Under 37 C.F.R. § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

Any other fee required for such Petition for Extension of Time and any other fee required by this document pursuant to 37 C.F.R. §§ 1.16 and 1.17, other than the issue fee,

and not submitted herewith should be charged to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260. Any refund should be credited to the same account.

Respectfully submitted,

By: _____

Michael J DeHaemer, Jr.
Registration No. 39,164
Attorney for Applicant

MJD:pm:bar

SIDLEY AUSTIN BROWN & WOOD LLP
717 N. Harwood, Suite 3400
Dallas, Texas 75201
Direct: (214) 981-3335
Main: (214) 981-3300
Facsimile: (214) 981-3400
November 18, 2004